

SANYO

No. 4915A

LC35256AM, AT-10LV/12LV/15LV**256K (32768 words × 8 bits) SRAM
with \overline{OE} and \overline{CE} Control Pins**

Overview

The LC35256AM, AT-10LV/12LV/15LV are asynchronous silicon-gate CMOS SRAMs with a 32K-word by 8-bit organization and a 6-transistor structure full-CMOS type memory cell. The LC35256AM, AT-10LV/12LV/15LV feature an ultralow voltage operation, a low operating current and an ultralow standby current. The LC35256AM, AT-10LV/12LV/15LV control signal inputs include an \overline{OE} input for high-speed memory access and a \overline{CE} (chip enable) input for device selection. Thus these products are optimal for systems that require low power and battery backup, and they allow memory system capacity to be expanded easily. The LC35256AM, AT-10LV/12LV/15LV ultralow standby current means that capacitor backup is also possible. These products feature 3 V operation to support 3 V power supply systems and a battery operation function that allows directly connected battery drive.

Features

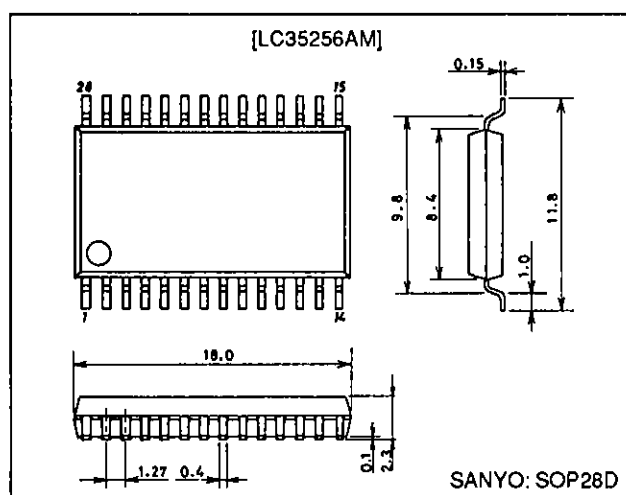
- Power supply voltage range: 2.0 to 3.6 V
 - 3 V operation: 2.7 to 3.6 V
 - Battery operation: 2.0 to 3.6 V
- Access times
 - 3 V operation
 - LC35256AM, AT-10LV: 100 ns (max.)
 - LC35256AM, AT-12LV: 120 ns (max.)
 - LC35256AM, AT-15LV: 150 ns (max.)
 - Battery operation
 - LC35256AM, AT-10LV: 200 ns (max.)
 - LC35256AM, AT-12LV: 240 ns (max.)
 - LC35256AM, AT-15LV: 300 ns (max.)
- Standby current: 0.8 μ A ($T_a \leq 60^\circ\text{C}$)
4.0 μ A ($T_a \leq 85^\circ\text{C}$)
- Operating temperature range: -40 to $+85^\circ\text{C}$
- Data retention power supply voltage: 2.0 to 3.6 V
- Input level: CMOS compatible
($0.8 V_{CC}/0.2 V_{CC}$)
- 28-pin SOP (450 mil) plastic package: LC35256AM Series
- 28-pin TSOP (TYPE-I) plastic package: LC35256AT Series

- Shared I/O pins, 3-state outputs
- No clock required (completely static circuits)

Package Dimensions

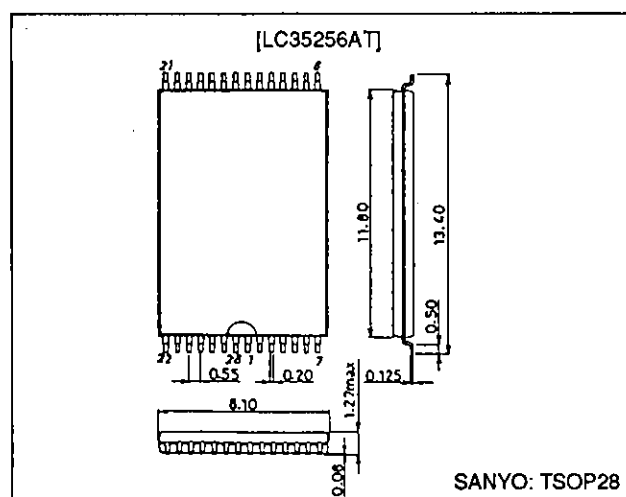
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3187-SOP28D



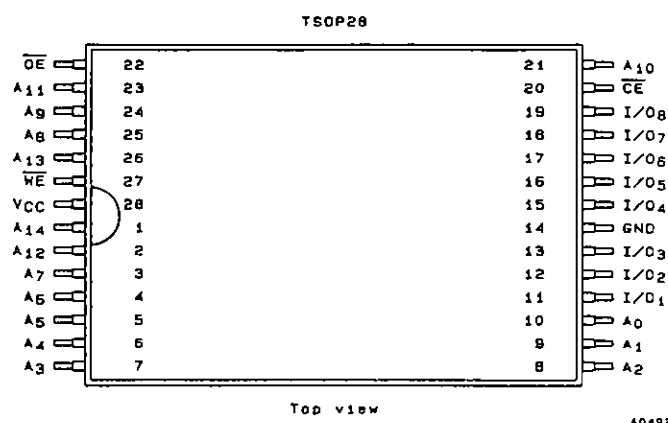
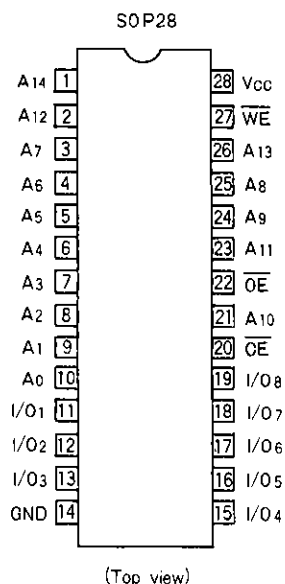
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3221-TSOP28

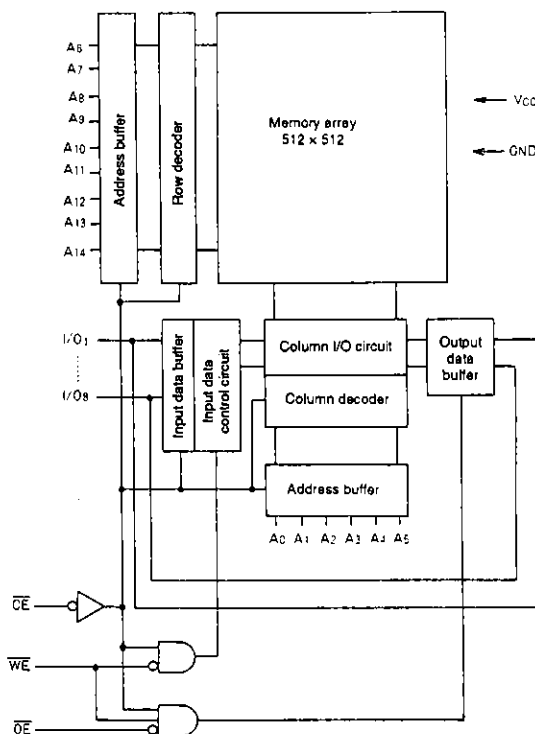
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Pin Assignment



Block Diagram



Pin Functions

A ₀ to A ₁₄	Address input
WE	Read/write control input
OE	Output enable input
CE	Chip enable input
I/O ₁ to I/O ₈	Data I/O
V _{CC} , GND	Power, ground

Truth Table

Mode	CE	OE	WE	I/O	Current drain
Read cycle	L	L	H	Data output	I _{CCA}
Write cycle	L	X	L	Data input	I _{CCA}
Output disable	L	H	H	High impedance	I _{CCA}
Deselect	H	X	X	High impedance	I _{CCS}

X: Either a high or low level

Specifications

Absolute Maximum Ratings*1

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	$V_{CC\ max}$		4.6	V
Input pin voltage	V_{IN}		-0.3^{*2} to $V_{CC} + 0.3$	V
I/O pins voltage	V_{IO}		-0.3 to $V_{CC} + 0.3$	V
Operating temperature	T_{opr}		-40 to $+85$	°C
Storage temperature	T_{stg}		-55 to $+125$	°C

Note: 1. A minimum value of -2.0 V is allowable for pulse widths under 30 ns.

2. Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation should be restricted to DC Allowable Operating Ranges. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

Input/Output Capacitances at $T_a = 25^{\circ}\text{C}$, $f = 1\text{ MHz}$

Parameter	Symbol	Conditions	min	typ	max	Unit
I/O pin capacitance	C_{IO}	$V_{IO} = 0\text{ V}$		6	10	pF
Input pin capacitance	C_I	$V_{IN} = 0\text{ V}$		6	10	pF

Note: These values are sampled values, and are not measured for all products.

3 V Operation

DC Recommended Operating Ranges at $T_a = -40$ to $+85^{\circ}\text{C}$, $V_{CC} = 2.7$ to 3.6 V

Parameter	Symbol	Conditions	min	typ	max	Unit
Supply voltage	V_{CC}		2.7	3.0	3.6	V
Input voltage	V_{IH}		$0.8 V_{CC}$		$V_{CC} + 0.3$	V
	V_{IL}		-0.3^{*}		$0.2 V_{CC}$	V

Note: * A minimum value of -2.0 V is allowable for pulse widths under 30 ns.

DC Electrical Characteristics at $T_a = -40$ to $+85^{\circ}\text{C}$, $V_{CC} = 2.7$ to 3.6 V

Parameter	Symbol	Conditions	min	typ*	max	Unit
Input leakage current	I_{LI}	$V_{IN} = 0$ to V_{CC}	-1.0		$+1.0$	μA
Output leakage current	I_{LO}	$V_{CE} = V_{IH}$ or $V_{OE} = V_{IH}$ or $V_{WE} = V_{IL}$, $V_{IO} = 0$ to V_{CC}	-1.0		$+1.0$	μA
Output high level voltage	V_{OH1}	$I_{OH1} = -2.0\text{ mA}$	$V_{CC} - 0.4$			V
	V_{OH2}	$I_{OH2} = -100\text{ }\mu\text{A}$	$V_{CC} - 0.1$			V
Output low level voltage	V_{OL1}	$I_{OL1} = 2.0\text{ mA}$			0.4	V
	V_{OL2}	$I_{OL2} = 100\text{ }\mu\text{A}$			0.1	V
Operating current	CMOS inputs	I_{CCA2}	$V_{CE} = V_{IL}$, $I_{IO} = 0\text{ mA}$, $V_{IN} = V_{IH}$ or V_{IL}		1.2	mA
		I_{CCA3}	$V_{CE} = V_{IL}$, $V_{IN} = V_{IH}$ or V_{IL} , $I_{IO} = 0\text{ mA}$, duty 100%	min		
				cycle		
				1 μs cycle		
Standby current	$V_{CC} - 0.2\text{ V}$ / 0.2 V inputs	I_{CCS1}	$V_{CE} \geq V_{CC} - 0.2\text{ V}$, $V_{IN} = 0$ to V_{CC}	$T_a \leq 25^{\circ}\text{C}$	0.01	
				$T_a \leq 60^{\circ}\text{C}$		0.8
				$T_a \leq 85^{\circ}\text{C}$		4.0
	CMOS inputs	I_{CCS2}	$V_{CE} = V_{IH}$, $V_{IN} = 0$ to V_{CC}			0.4

Note: * Reference values when $V_{CC} = 3\text{ V}$ and $T_a = 25^{\circ}\text{C}$

AC Electrical Characteristics at $T_a = -40$ to $+85^{\circ}\text{C}$, $V_{CC} = 2.7$ to 3.6 V

AC test conditions

Input pulse voltage level: $0.2 V_{CC}$ to $0.8 V_{CC}$

Input rise and fall times: 5 ns

Input and output timing levels: $1/2 V_{CC}$

Output load: 30 pF (including the jig capacitance)

Read Cycle

Parameter	Symbol	LC35256AM, AT						Unit
		-10LV		-12LV		-15LV		
		min	max	min	max	min	max	
Read cycle time	t _{RC}	100		120		150		ns
Address access time	t _{AA}		100		120		150	ns
CE access time	t _{CA}		100		120		150	ns
OE access time	t _{OA}		50		60		70	ns
Output hold time	t _{OH}	10		10		10		ns
CE output enable time	t _{COE}	10		10		10		ns
OE output enable time	t _{OOE}	5		5		5		ns
CE output disable time	t _{COD}		35		40		40	ns
OE output disable time	t _{OOD}		30		35		35	ns

Write Cycle

Parameter	Symbol	LC35256AM, AT						Unit
		-10LV		-12LV		-15LV		
		min	max	min	max	min	max	
Write cycle time	t _{WC}	100		120		150		ns
Address setup time	t _{AS}	0		0		0		ns
Write pulse width	t _{WP}	80		90		100		ns
CE setup time	t _{CW}	90		100		110		ns
Write recovery time	t _{WR}	0		0		0		ns
CE write recovery time	t _{WR1}	0		0		0		ns
Data setup time	t _{DS}	50		55		60		ns
Data hold time	t _{DH}	0		0		0		ns
CE data hold time	t _{DH1}	0		0		0		ns
WE output enable time	t _{WOE}	5		5		5		ns
WE output disable time	t _{WOD}		35		40		40	ns

Battery Operation

DC Recommended Operating Ranges at $T_a = -40$ to $+85^\circ\text{C}$, $V_{CC} = 2.0$ to 3.6 V

Parameter	Symbol	Conditions	min	typ	max	Unit
Supply voltage	V_{CC}		2.0	3.0	3.6	V
Input voltage	V_{IH}		$0.8 V_{CC}$		$V_{CC} + 0.3$	V
	V_{IL}		-0.3^*		$0.2 V_{CC}$	V

Note: * A minimum value of -1.0 V is allowable for pulse widths under 30 ns.DC Electrical Characteristics at $T_a = -40$ to $+85^\circ\text{C}$, $V_{CC} = 2.0$ to 3.6 V

Parameter		Symbol	Conditions		min	typ*	max	Unit
Input leakage current		I_{LI}	$V_{IN} = 0$ to V_{CC}		-1.0		+1.0	μA
Output leakage current		I_{LO}	$V_{CE} = V_{IH}$ or $V_{OE} = V_{IH}$ or $V_{WE} = V_{IL}$, $V_{IO} = 0$ to V_{CC}		-1.0		+1.0	μA
Output high level voltage		V_{OH1}	$I_{OH1} = -0.5$ mA		$V_{CC} - 0.2$			V
		V_{OH2}	$I_{OH2} = -100$ μA		$V_{CC} - 0.1$			V
Output low level voltage		V_{OL1}	$I_{OL1} = 0.5$ mA				0.2	V
		V_{OL2}	$I_{OL2} = 100$ μA				0.1	V
Operating current	CMOS inputs	I_{CCA2}	$V_{CE} = V_{IL}$, $I_{IO} = 0$ mA, $V_{IN} = V_{IH}$ or V_{IL}				1.2	mA
		I_{CCA3}	$V_{CE} = V_{IL}$, $V_{IN} = V_{IH}$ or V_{IL} , $I_{IO} = 0$ mA, duty 100%	min cycle	LC35256AM, AT-10LV	7.0	10.0	mA
					LC35256AM, AT-12LV	6.0	8.0	
					LC35256AM, AT-15LV	5.0	7.0	
		1 μs cycle			1.5	2.5		
Standby current	$V_{CC} - 0.2$ V/ 0.2 V inputs	I_{CCS1}	$V_{CE} \geq V_{CC} - 0.2$ V, $V_{IN} = 0$ to V_{CC}	$T_a \leq 25^{\circ}C$		0.01		μA
				$T_a \leq 60^{\circ}C$			0.8	
				$T_a \leq 85^{\circ}C$			4.0	
		CMOS inputs	I_{CCS2}	$V_{OE} = V_{IH}$, $V_{IN} = 0$ to V_{CC}				0.4

Note: * Reference values when $V_{CC} = 3$ V and $T_a = 25^\circ\text{C}$

AC Electrical Characteristics at Ta = -40 to +85°C, V_{CC} = 2.0 to 3.6 V

AC test conditions

Input pulse voltage level: 0.2 V_{CC} to 0.8 V_{CC}

Input rise and fall times: 10 ns

Input and output timing levels: 1/2 V_{CC}

Output load: 30 pF (including the jig capacitance)

Read Cycle

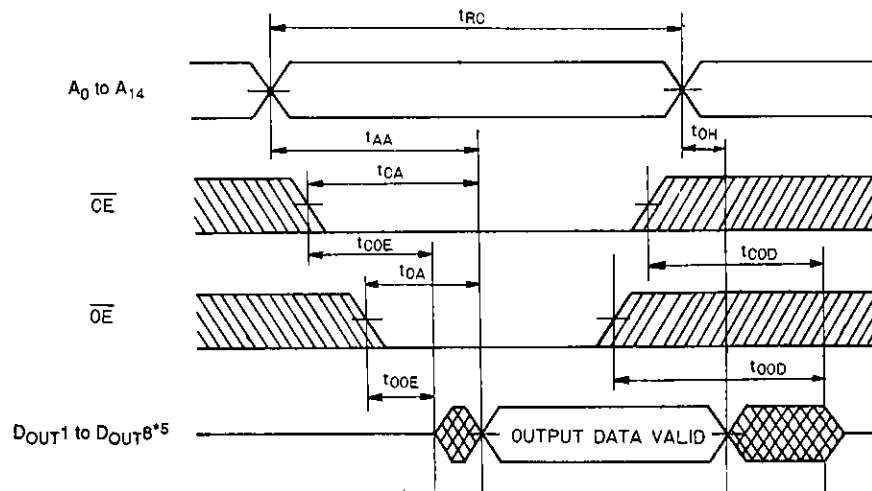
Parameter	Symbol	LC35256AM, AT						Unit
		-10LV		-12LV		-15LV		
		min	max	min	max	min	max	
Read cycle time	t _{RC}	200		240		300		ns
Address access time	t _{AA}		200		240		300	ns
$\overline{\text{CE}}$ access time	t _{CA}		200		240		300	ns
$\overline{\text{OE}}$ access time	t _{OA}		100		120		150	ns
Output hold time	t _{OH}	10		10		10		ns
$\overline{\text{CE}}$ output enable time	t _{COE}	10		10		10		ns
$\overline{\text{OE}}$ output enable time	t _{OOE}	5		5		5		ns
$\overline{\text{CE}}$ output disable time	t _{COD}		70		80		80	ns
$\overline{\text{OE}}$ output disable time	t _{OOD}		60		70		75	ns

Write Cycle

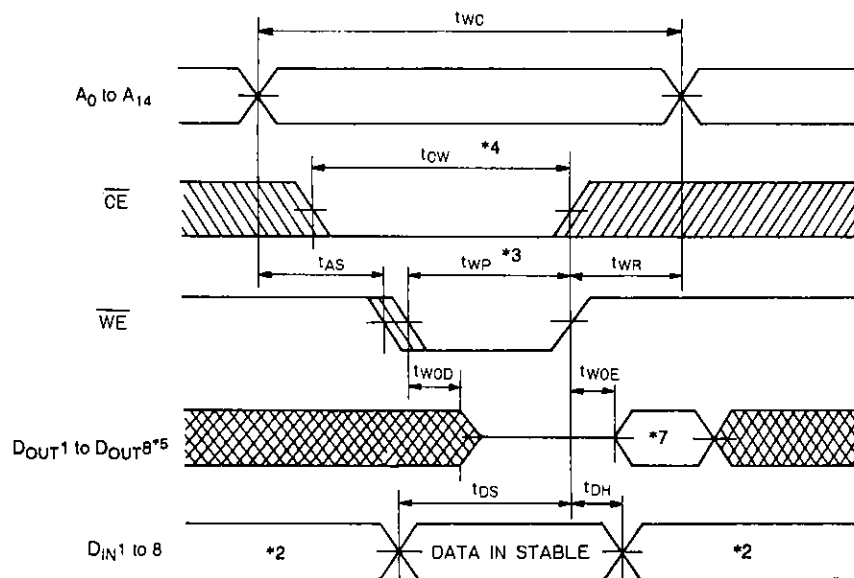
Parameter	Symbol	LC35256AM, AT						Unit
		-10LV		-12LV		-15LV		
		min	max	min	max	min	max	
Write cycle time	t _{WC}	200		240		300		ns
Address setup time	t _{AS}	0		0		0		
Write pulse width	t _{WP}	160		180		200		
$\overline{\text{CE}}$ setup time	t _{CW}	180		200		220		
Write recovery time	t _{WR}	0		0		0		
$\overline{\text{CE}}$ write recovery time	t _{WR1}	0		0		0		
Data setup time	t _{DS}	100		110		120		
Data hold time	t _{DH}	0		0		0		
$\overline{\text{CE}}$ data hold time	t _{DH1}	0		0		0		
$\overline{\text{WE}}$ output enable time	t _{WOE}	5		5		5		
$\overline{\text{WE}}$ output disable time	t _{WOD}		70		80		80	

Timing Chart

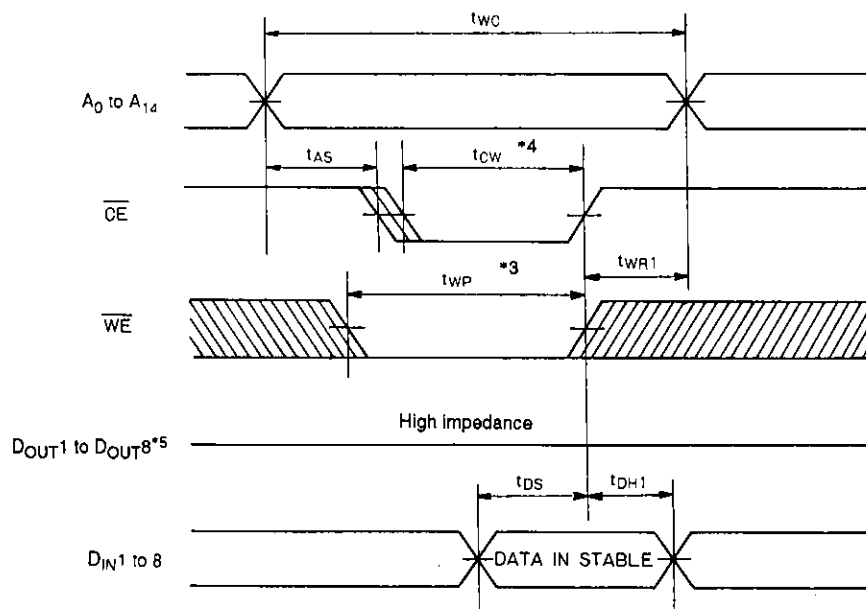
Read Cycle*1



Write Cycle 1 (\overline{WE} write)*6



Write Cycle 2 (\overline{CE} write)*6



Note: 1. Set \overline{WE} high during the read cycle.

2. An external reverse phase signal must not be applied when D_{OUT} is in the output state.

3. t_{WP} is defined to be the period, when both \overline{CE} and \overline{WE} are low, from the fall of \overline{WE} to the point where the first of either \overline{CE} or \overline{WE} rises.

4. t_{CW} is defined to be the period, when both \overline{CE} and \overline{WE} are low, from the fall of \overline{CE} to the point where the first of either \overline{CE} or \overline{WE} rises.

5. D_{OUT} goes to the high impedance state when either \overline{OE} is high, \overline{CE} is high, or \overline{WE} is low.

6. \overline{OE} must be set either high or low during the write cycle.

7. D_{OUT} has the same phase as the write data for the current write cycle.

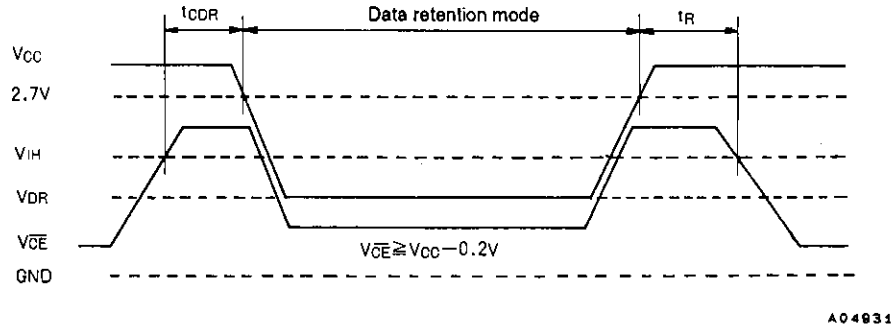
Data Retention Characteristics at Ta = -40 to +85°C

3 V Operation

Parameter	Symbol	Conditions	min	typ	max	Unit
Data retention supply voltage	V_{DR}	$V_{CE} \geq V_{CC} - 0.2 V$	2.0		3.6	V
Chip enable setup time	t_{CDR}		0			ns
Chip enable hold time	t_R		t_{RC}^*			ns

Note: * t_{RC} is the read cycle time.

Data Retention Waveform



Battery Operation

Parameter	Symbol	Conditions	min	typ	max	Unit
Data retention supply voltage	V_{DR}	$V_{CE} \geq V_{CC} - 0.2 V$	2.0		3.6	V

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